REMARKS/ARGUMENTS

The following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

Drawings

Figure 1 has been amended as requested by the Examiner.

35 U.S.C. § 102 Rejections

Examiner rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,755,939 to Watson (hereinafter "Watson").

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). [MPEP § 2131]

> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). [MPEP § 2131]

Claim 1 reads as follows:

A method comprising:
removing a work item of a plurality of work items from an enabled expansion bus schedule data structure;
generating a coherency signal *utilizing an expansion bus host controller* in response to removing said work item from said enabled expansion bus schedule data structure; and
reclaiming said work item *whenever* said coherency signal is generated.
(emphasis added)

Watson does not include all the limitations of claim 1, and therefore does not anticipate claim 1. Specifically, Watson discloses garbage collection in a computer system (Col. 1, lines 5-6). Watson further discloses a means of

reclaiming memory cells which are no longer being used by the programs to which they are allocated, so that they can be re-allocated for further use (Col. 1, lines 21-28). The Examiner asserts that Watson's disclosure of reducing a reference count of a cell when a pointer to that cell is destroyed (Col. 2, lines 44-46) in part anticipates claim 1. This disclosure is limited to memory cells, however, and Watson is generally directed toward memory management and devices (Col. 2, lines 23-28). Watson does not disclose generating a coherency signal *utilizing an expansion bus host controller*, as in claim 1. Instead, Watson discloses reducing a reference count of a memory cell when a pointer is destroyed. Nowhere does Watson disclose an expansion bus host controller, or anything similar. Therefore, Watson does not anticipate claim 1.

Further, Watson does not disclose generating a coherency signal and reclaiming said work item *whenever* said coherency signal is generated. Watson discloses that cells are only reclaimed when their reference count equals zero (Col. 2, lines 47-48). So, a pointer may be destroyed, and the reference count of the memory cell to which it is pointing does not become zero as a result (for example, when more than one pointer is pointing to the cell, the remaining pointer would leave the cell with a non-zero reference count). Since the memory cell is not reclaimed, even though the pointer is destroyed, Watson does not disclose the claimed limitation. As a result, Watson does not anticipate claim 1.

Examiner rejected claims 1 and 11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,502,111 to Dussud (hereinafter "Dussud").

Dussud discloses automatic reclamation of allocated memory or garbage collection. Dussud discloses marking a memory object to indicate that the memory object is allocated and still reachable (Col. 2, lines 21-28, Col. 8, lines 36-

37). After the memory objects are marked, a sweep is performed to reclaim the dead memory (Col. 8, lines 37-40).

Similar to Watson, Dussud does not disclose generating a coherency signal *utilizing an expansion bus host controller*. Instead, also like Watson, Dussud discloses operations performed in memory using memory devices. As a result, since Dussud does not include all the elements of this limitation, claim 1 is not anticipated by Dussud.

Claim 1 also includes a limitation of generating a coherency signal utilizing an expansion bus host controller *in response to removing said work item* from said enabled expansion bus schedule data structure. According to the Examiner, Dussud discloses this limitation by disclosing that when a memory object is modified, a bit flag is set to indicate such a modification (Col. 9, lines 7-9). However, modifying a memory object is different from removing a work item. Further, the bit flag is set while the garbage collection is occurring, and while the garbage collector module is marking reachable objects (Col. 3, lines 15-20). Setting the bit flag is distinct from marking the reachable memory objects. The bit flag does not indicate which memory objects will be reclaimed, only which memory objects need to be examined again to determine whether they should be marked, since they have been modified during the scan. So, even if setting the bit flag is considered equivalent with generating a coherency signal, it is still not done in response to *removing* a memory object, but rather in response to a *modification* of a memory object.

Dussud does disclose reclaiming memory during a garbage collection process (Col. 8, lines 37-40). However, the garbage collection process is not initiated in response to the removal of a memory object. Instead, Dussud discloses that the garbage collection process is typically initiated when a number

of allocated objects exceeds a predetermined threshold (Col. 1, line 65 – Col. 2, line 3). As a result, as taught by Dussud, the garbage collection process does not begin in response to a memory object being removed. Instead, as Dussud discloses it, the addition of a memory object triggers the process, since the addition of a memory object would be necessary to add enough allocated memory objects to surpass the predetermined threshold. Therefore, Dussud does not disclose generating a coherency signal utilizing an expansion bus host controller *in response to removing said work item*, and does not anticipate claim 1.

Dussud's disclosure of marking reachable memory objects is also not equivalent to the claimed limitation of generating a coherency signal utilizing an expansion bus host controller in response to removing a work item. First, the memory objects marked by Dussud are those that are still being used by the programs to which they are allocated, so they have not been removed. Further, as stated above, the garbage collection process is initiated in response to a total number of allocated memory objects reaching a predetermined threshold. So, since the marking begins in response to reaching a threshold, the claimed limitation of generating a coherency signal in response to removing a work item is not taught by Dussud.

Claim 11 includes limitations similar to those discussed above regarding claim 1. As a result, since claim 1 is not anticipated by Dussud, claim 11 is also not anticipated by Dussud.

Examiner rejected claims 21, 22, and 27 under 35 U.S.C. § 102(b) as being anticipated by *Universal Host Controller Interface (UHCI) Design Guide*, Rev. 1.1, by Intel (hereinafter "Intel")

Claim 21 includes a limitation of a status register including a status signal bit to notify an expansion bus host controller driver *that a work item may be reclaimed*. The USBSTS status register taught by Intel indicates pending interrupts and various states on a Host Controller (see Page 13, Section 2.1.2). Intel lists several different values for the register, none of which mention indicating that a work item may be reclaimed. Moreover, Intel does not disclose reclaiming work items, so Intel cannot anticipate claim 21, since Intel does not include all the limitations of claim 21.

Claim 27 includes a limitation similar to the above limitation discussed regarding claim 21. Since claim 21 is not anticipated by Intel, claim 27 is also not anticipated by Intel.

35 U.S.C. § 103(a) Rejections

Examiner rejected claims 2-4 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Watson in view of Intel.

Claims 2-4 and 10 depend from claim 1, and therefore include all the limitations of claim 1. As mentioned above, claim 1 is not anticipated by Watson. Intel does not add the missing limitations of either claim 1 as discussed above. Therefore, claims 2-4 and 10 are patentable over Watson and Intel.

Examiner rejected claims 2-5, 10, 12-15, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Dussud in view of Intel.

Claims 2-5, 10, 12-15, and 20 depend from the independent claims 1 or 11, and therefore include all the limitations of those independent claims. As mentioned above, claims 1 and 11 are not anticipated by Dussud. Intel does not

add the missing limitations of claim 1, and, claims 2-5, 10, 12-15, and 20 are therefore patentable over Dussud and Intel.

Examiner rejected claims 6-9, and 16-19 under 35 U.S.C. § 103(a) as being unpatentable over Dussud in view of Intel as applied to claims 5 and 15 above, and further in view of U.S. Patent No. 6,128,654 to Runaldue, et al. (hereinafter "Watson").

Claims 6-9 and 16-19 depend from the independent claims 1 or 11, and therefore include all the limitations of those independent claims. As mentioned above, claims 1 and 11 are not anticipated by Dussud. Neither Intel nor Runaldue add the missing limitations of claim 1, and claims 6-9 and 16-19 are therefore patentable over Dussud, Intel, and Runaldue.

Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Watson in view of U.S. Patent Application Publication No. 2002/0133533 to Czajkowski, et al. (hereinafter "Czajkowski").

Claim 11 includes limitations similar to those discussed above regarding Claim 1 and Watson. As a result, since claim 1 is not anticipated by Watson, and Czajkowski does not add the missing limitations of claim 11 as discussed above, claim 11 is patentable over Watson and Czajkowski.

Examiner rejected claims 12-14 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Watson in view of Czajkowski as applied to claim 1 above, and further in view of Intel.

Claims 12-14 and 20 depend from claim 11, and therefore include all the limitations of claim 11. As mentioned above, claim 11 is patentable over Watson

and Czajkowski. Intel does not add the missing limitation of claim 11, and as a result, claims 12-14 and 20 are patentable over Watson, Czajkowski, and Intel.

Examiner rejected claims 23-26 and 28-30 under 35 U.S.C. § 103(a) as being unpatentable over Intel in view of Runaldue.

Claims 23-26 and 28-30 depend from the independent claims 21 and 27, and therefore include all the limitations of those independent claims. As mentioned above, claims 21 and 27 are not anticipated by Intel. Runaldue does not add the missing limitations of claims 21 and 27 discussed above. Therefore, claims 23-26 and 28-30 are patentable over Intel and Runaldue.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Arlen Hartounian at (408) 720-8300, x352.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 7/06/04

Arlen M. Hartounian
Reg. No. 52,997

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300